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5 at least one emitter to generate an electron beam, the emitter having a silicon-based dielectric layer having a thickness between about 250 to 5000 Angstroms, and a cathode layer disposed on the silicon-based dielectric layer, the at least one emitter subjected to an annealing process to create nano-porous openings in the cathode layer;

 a lens for focusing the electron beam to create a focused beam; and
 a storage medium in close proximity to the at least one emitter, the storage medium having a storage area being in one of a plurality of states to represent the information stored in that storage area;

10 such that:

 an effect is generated when the focused beam bombards the storage area;

 the magnitude of the effect depends on the state of the storage area;
 and

15 the information stored in the storage area is read by measuring the magnitude of the effect.

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17. (Amended) An emitter, comprising:

 an electron supply layer;

20 an insulator layer formed on the electron supply layer and having an opening defined within;

 a silicon-based dielectric layer formed on the electron supply layer in the opening and further disposed over the insulator layer; and

 a cathode layer formed on the silicon-based dielectric layer;

25 wherein the emitter has been subjected to an annealing process to create nano-porous openings in the cathode layer and to increase the supply of electrons tunneled from the electron supply layer to the cathode layer for energy emission.

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29. (Amended) An emitter, comprising:

30 an electron supply surface;

 an insulator layer formed on the electron supply surface and having a first opening defined within;

 a silicon-based dielectric layer formed on the electron supply layer within the first, opening and further disposed on the insulator layer;

an adhesion layer disposed on the silicon-based dielectric layer, the adhesion layer defining a second opening aligned with the first opening;

A8 a conductive layer disposed on adhesion layer and defining a third opening aligned with the first and second openings; and

5 a cathode layer disposed on the silicon-based dielectric layer and portions of the conductive layer, wherein the portion of the cathode layer on the silicon-based dielectric layer is an electron-emitting surface having nano-porous openings.

A9 10 36. (Amended) An emitter, comprising:

an emitting surface having a first area and nano-porous openings;

a first chamber having substantially parallel sidewalls interfacing to the emitting surface; and

15 a second chamber interfacing to the first chamber and having sidewalls diverging to an opening having a second area larger than the first area.

A10 43. (Amended) An integrated circuit, comprising:

a conductive surface to provide an electron supply;

at least one emitter formed on the electron supply including,

20 an insulator layer having at least one opening to define the location and shape of the at least one flat emitter device,

a silicon-based dielectric layer disposed within the at least one opening of the insulator layer and further disposed over the insulator layer;

a conductive layer disposed over the silicon-based dielectric layer,

25 the conductive layer having at least one opening in alignment with the at least one opening; and

a cathode layer disposed over the silicon-based dielectric layer and partially over the conductive layer, the cathode layer having nano-porous openings.

30 Please cancel claims 48-63 without prejudice.